AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 13, line 25 with the following amended paragraph:

The second stage includes a multiplexer circuit 196, which has inputs A, B, C, S_A, S_B, S_C and an output, out. The A, B, C, inputs of multiplexer 196 receive the $aa_{1,-1}$, a_2, a_{-2} signals 192. The S_A, S_B, S_C, inputs receive the $s_{1,-1}$, s_2, s_{-2} signals 198. The output of the multiplexer circuit 196, OUT, supplies the partial product bit PPj_i, on a line 200. The operation of multiplexer circuit 196 is as follows. If $s_{1,-1}$ is asserted, then the partial product bit PPj_i has a logic state equal to the logic state of $aa_{1,-1}$. If s_2 is asserted, then the partial product bit PPj_i has a logic state equal to the logic state of aa_2. If s_{-2} is asserted, then the partial product bit PPj_i has a logic state equal to the logic state of aa_{-2}.

Please replace the paragraph beginning on page 17, line 25 with the following amended paragraph:

FIG. 10 shows one embodiment of the transmission gates 350A-350C. In this embodiment, the input terminal ("in") of the transmission gate is connected to a source terminal 354 of a p-channel MOSFET 356 and a source terminal 358 of an n-channel MOSFET 360. The control terminal ("control") of the transmission gate is connected to a gate 362 of the n-channel MOSFET 360 and supplied to an inverter 364, which generates a signal $NOT(s_{1,-1})$ supplied to a gate 366 of the p-channel MOSFET 356. The drain 368 of the p-channel MOSFET 356 and the drain 370 of the n-channel MOSFET 360 are connected to the output terminal ("out") of the transmission gate.

Please replace the paragraph beginning on page 18, line 16 with the following amended paragraph:

In this embodiment, the partial product generator 560 has k partial product bit generators in all, four of which are shown, i.e., 170A-170D. The partial product bit generator 170A receives bits

b_{j+1}, b_j, b_{j-1} of the multiplier B and receives bit a_0 of the multiplicand A and generates bit PPj_0 of the partial product PPj. The partial product bit generator 170B receives bits b_{j+1}, b_j, b_{j-1} of the multiplier B and bits a_1, a_0 of the multiplicand A and generates bit PPj_1 of the partial product PPj. The partial product bit generator 170C receives bits b_{j+1}, b_j, b_{j-1} of the multiplier B and bits ~~a_{n-1}, a_{n-2}~~ a_{n-2}, a_{n-3} of the multiplicand A and generates bit PPj_{k-2} of the partial product PPj. The partial product bit generator 170D receives bits b_{j+1}, b_j, b_{j-1} of the multiplier B and bits ~~a_n, a_{n-1}~~ a_{n-1}, a_{n-2} of the multiplicand A and generates bit PPj_{k-1} of the partial product PPj.